

EV372467728

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 09/512,149  
Filing Date .... February 23, 2000  
Inventor .... Vishnu K. Agarwal  
Assignee .... Micron Technology, Inc.  
Group Art Unit .... 2814  
Examiner .... M. Pizarro Crespo  
Attorney's Docket No. .... MI22-1322

Title: Integrated Circuitry Including a Capacitor with an Amorphous and a Crystalline High K Capacitor Dielectric Region

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

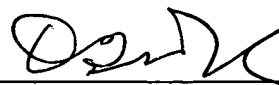
References -- See Attached Form PTO-1449

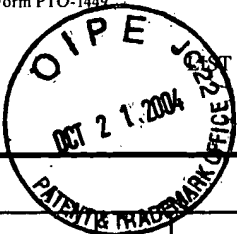
The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449 and a copy of which is attached. No admission is made regarding whether the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 10-31-04

By:   
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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1322		SERIAL NO. 09/512,149	
 LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Vishnu K. Agarwal et al.			
				FILING DATE February 23, 2000		GROUP 2814	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	5,753,547	05/19/98	Ying				
AB	6,204,203 B1	03/20/01	Narwankar et al.				
AC	5,973,911	10/26/99	Nishioka				
AD	6,727,143	04/04	Hui et al.				
AE							
AF							
AG							
AH							
AI							
AJ							
AK							
AL							
FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
AM							
AN							
AO							
AP							
AQ							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
AR							
AS							
AT							
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							